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Performance comparison of ripple carry array and carry save array multiplier using clock signal

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Abstract

This paper is on study and developing an Efficient Fast and Low Power Multiplier. Multiplier being core part of arithmetic processing unit they are in high demand on its speed and low power consumption. Also they require more hardware resources and processing time than addition and subtraction. The design emphasis seems to be shifted from optimizing conventional delay time area size to minimizing power dissipation while maintaining high performance. As power, area and delay and complexity are important considerations for VLSI design a comparative performance analysis may act as a direction finder for low power requirement and high speed using algorithms for multiplier design that are proposed for fast multiplication.

Index Terms: *Reduction process, different arrays, multipliers, clocked multiplier with display screens using VLSI.*

1. INTRODUCTION

With the growing scale of integration, large numbers of sophisticated signal processing systems are being implemented on a VLSI chip. While performance and Area are the two major design approaches, power consumption has become a critical concern in today's VLSI system design. The need for low-power VLSI system came from two main forces. One, with the steady growth of operating frequency and processing capacity per chip, large currents need to be delivered and heat due to large power consumption must be removed by proper cooling techniques. The other one, battery life in portable electronic devices is restricted. Low power design directly leads to chronic operation time in these portable devices. Multiplication is an essential operation in optimising algorithms which process signals. Multipliers have larger area, more latency and consume acceptable power. Therefore low-power multiplier design is necessary part in low power VLSI system design. At technology, physical, circuit and logic levels extensive work on low-power multipliers has been done. Multiplier being the slowest element in the system, the system's performance is generally determined by the performance of the multiplier. Moreover the area consumption is maximum. Therefore, optimization of the speed and area of the multiplier is the most important task.

II. RESEARCH APPROACH

The main objective of our project is to study and develop an Efficient Fast and Low Power Multiplier. To achieve this we had to go for faster and low power factor optimization. As we know that the fundamental building block of a multiplier is

ADDER circuit. Therefore we focus into The ADDERS first. We have studied the area occupied and the time delay required by different adders and concluded a proper relation between time and area complexity of all the adders under consideration.

III. MULTIPLICATION PROCESS AND REDUCTION OF PARTIAL PRODUCT

Multiplication consists of three steps: generating partial products (PPG), reducing partial products (PPR), and at last carry-propagate addition (CPA). Different multiplication algorithms vary in the implementation of PPG, PPR, and CPA

Step 1: Generation of Partial products

The first step is similar to normal binary multiplication used by us. This step will generate Partial products (PPs).

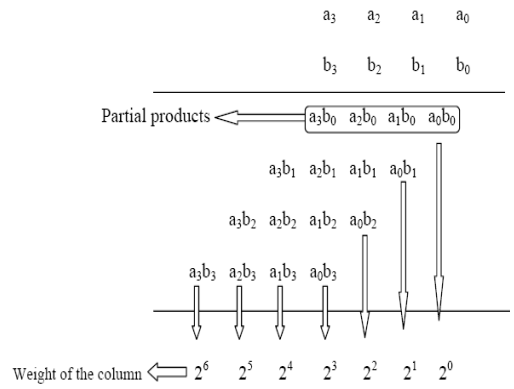


FIG 1: 4 Bit Multiplication Partial Product

Step 2: Reduction Stages:

Now the generated partial products are added using 'Half adders' and 'Full adders'. Following guide lines are to be followed in the addition process.

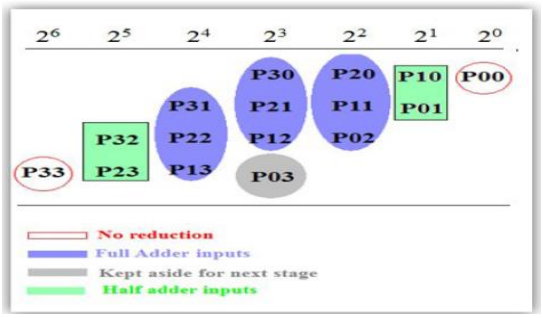


FIG 2: Use of Full Adders and Half Adders for Reduction of PPs

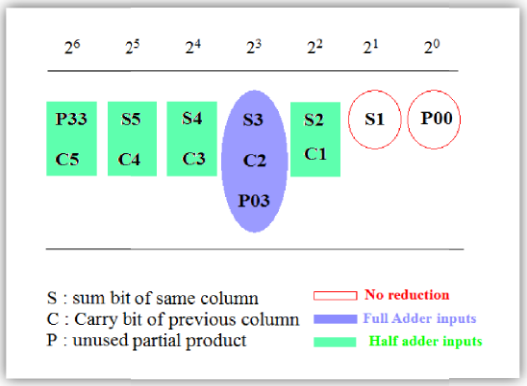


FIG 3: Second Level Of Reduction

IV. THE ADDERS

Addition serves as a building block for synthesis all other arithmetic operations. The binary adder structures become a very critical hardware unit after regarding the efficient implementation of an arithmetic unit. In this paper, qualitative evaluations of different binary adder architectures are studied. We have studied VHDL (Hardware Description Language) code for Ripple-carry adder and Carry-select adder to emphasize the common performance properties belonging to them. Considering delay, area complexity, we can categorize the binary adder architectures. The first class consists of the very slow ripple-carry adder with the smallest area. In the second class, carry-select adders with different levels have small area requirements and short computation times.

Ripple Carry Adders (RCA):

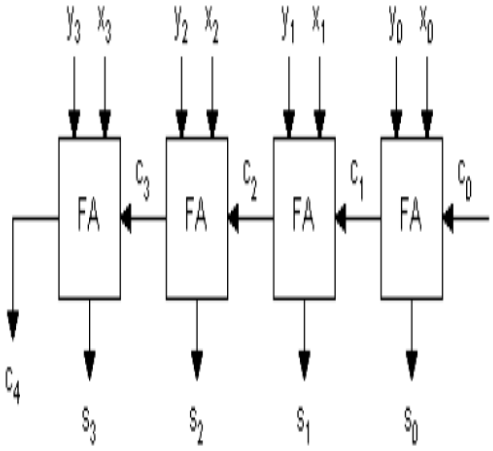


FIG 4: A 4-bit Ripple Carry Adder

The very well-known adder, ripple carry adder is composed by cascading full adders to make n-bit adder, as shown in figure4. It is made by cascading full adder blocks serially. The carry output of first stage is directly fed to the carry-input of the next stage. For an n-bit parallel adder it requires n full adders. But the disadvantage with this kind of adder is that it is not very efficient when large bit numbers are used and it also increases delay.

Carry Select Adders (CSLA):

In Carry select adder scheme, blocks of bits are added in two ways: one assuming a carry-in of 0 and the other with a carry-in of 1.This results in two recomputed sum and carry-out signal pair **(s0i-1:k , c0i ; s1i-1:k , c1i) ,** later as the block's true carry-in (**ck**) becomes known , the correct signal pairs are selected. Generally multiplexers are used to propagate carries.

- Because of multiplexer's larger area is required.
- Have a lesser delay than Ripple Carry Adders (**half delay of RCA**).
- As a result we always prefer Carry Select Adder while working with smaller no of bits.

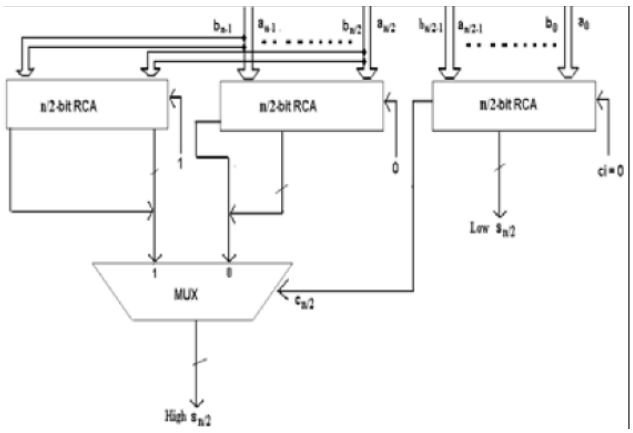


FIG 5: A Carry Select Adder with 1 Level Using n/2 Bit-RCA

ANALYSIS OF ADDERS

Here we are comparing 2 different adders ***Ripple Carry Adders***, ***Carry Select Adders.*** The basic purpose of our paper was to know the least delay and area required between different adders which will give us a clear picture of which adder suits best in design process of the low power array multiplier.

1. Considering the ***circuit area complexity*** in the adder architectures, the ***ripple-carry adder*** (RCA) is the most efficient one.

2. Considering the ***circuit delay time***, ***Carry Select*** Adder (CSLA) is the fastest one for every n-bit length, so has the shortest delay.

V. ARRAY MULTIPLIERS:

Conventional linear array multipliers consist of rows of carry save adders (CSA).In a linear array multiplier, as the data propagates down the array, one additional partial redundant is added by each row of CSA's. Hence we can conclude that the delay of an array multiplier is only dependent on depth of the array, and is not dependent on the partial product width. These linear array multipliers are also regular, comprising of replicated row of CSA's, their high performance and regular structure have made the use of array multipliers of VLSI

math co-processors and special purpose DSP chips in large area.

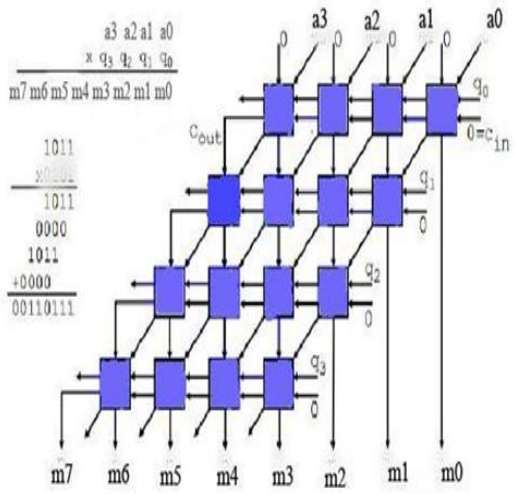


FIG 6: Array Multiplier

VI. RIPPLE CARRY MULTIPLIER

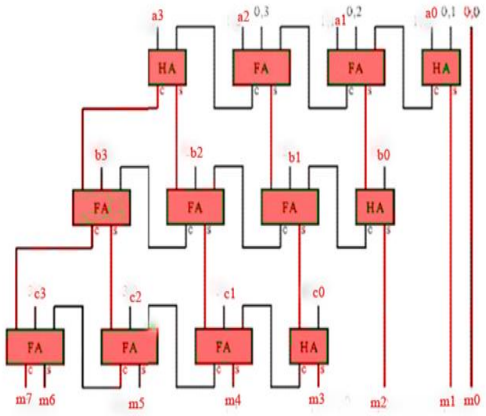


FIG 7: Ripple Carry Array Multiplier

The maximum delay is the path from either LSB input to the MSB of the product, and is the same (ignoring routing) regardless of the path taken. The delay is approximately 2n. This basic structure is simple to construct in FPGAs, but does not use logic efficiently in many FPGAs, and is hence larger and slower than application.

VII. CARRY SAVE ARRAY MULTIPLIERS:

We can use Carry save adder for adding each group of partial product terms instead of using Ripple carry adder (RCA), because RCA is the slowest adder among all other adders available. Figure 8 shows structure of carry save array multiplier to add each group of partial products in paralleled way. The algorithm for process of multiplication is the same. The only difference in them is the process of performing addition of final addition and partial products. Figure below shows the working of the multipliers while dealing continuous systems. When we apply clock to the same system, the change in output takes place.

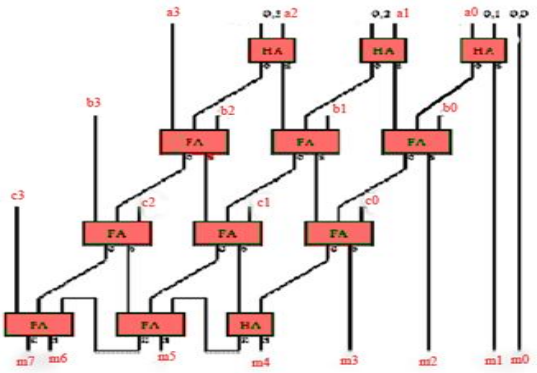


FIG 8: Carry save Array Multiplier

VIII. CLOCKED CARRY SAVE ARRAY MULTIPLIER:

FIG 9: Timing Response

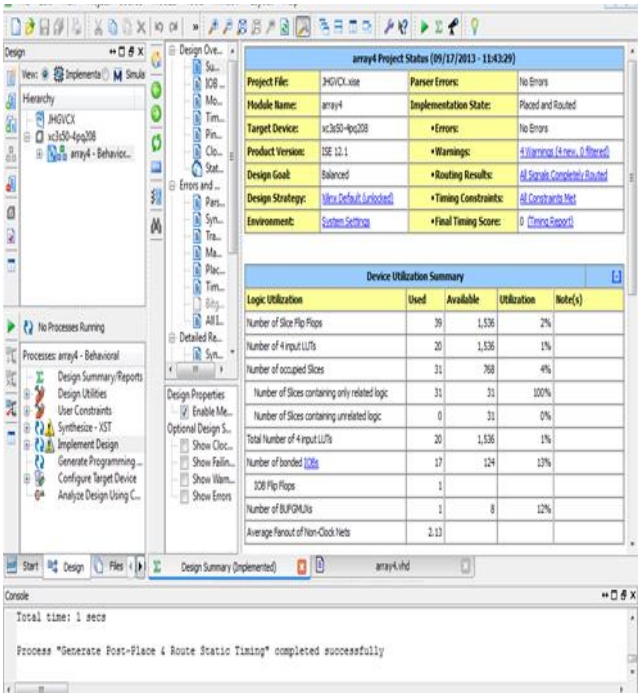


FIG 10: Area Response

The fig above shows the timing report and area report of the clocked array multiplier. The simulated design is as shown in FIG 11.

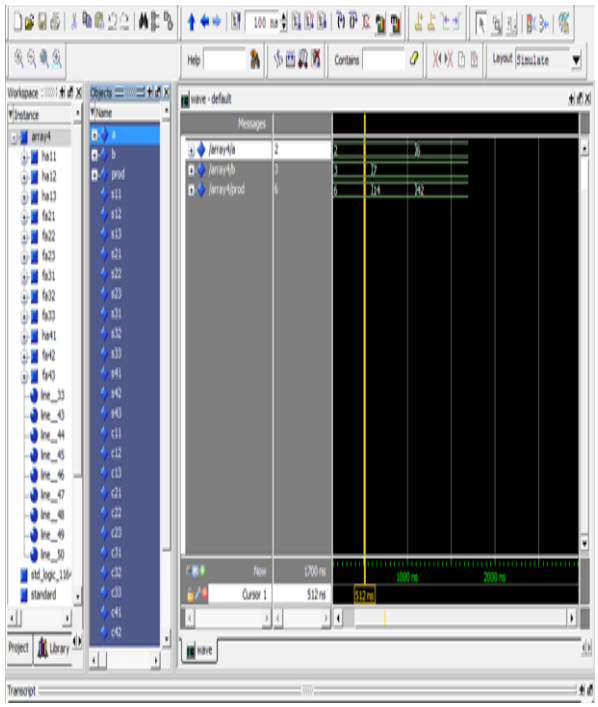
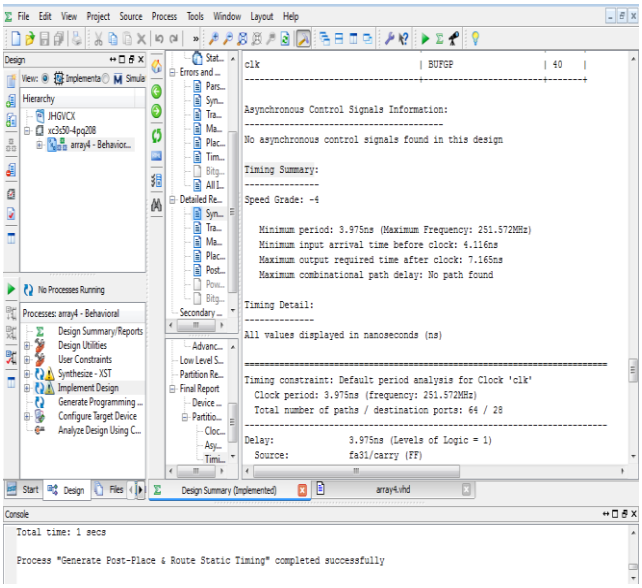


FIG 11: Simulated design



Comparing various multipliers with respect to area and delay we come to the conclusion that has been noted down in table as follows:

	Ripple Carry Array mul.	**Carry select Adder mul.**	**Clocked mul.**
Area	**31 LUTS**	**33 LUTS**	**20 LUTS**
Delay	**20.378ns**	**17.431ns**	**7.165ns**

IX. CONCLUSION:

After comparing various multipliers we found that the fastest and most efficient array multiplier is clocked carry save array multiplier with lowest area required.

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